What is claimed is:

1. An EEPROM having a memory transistor, said memory transistor comprising:

a drain region of a second conductivity type formed in a superficial layer of a semiconductor substrate of a first conductivity type, said drain region including an embedded layer and a drain side field moderating layer formed adjacent to said embedded layer;

a source region of the second conductivity type in the superficial layer of said semiconductor substrate;

a channel region between said drain region and said source region;

a gate insulating film formed on a surface of said semiconductor substrate;

a tunnel film formed in a part of said gate insulating film above said embedded layer;

a floating gate electrode formed above said tunnel film and said channel region and having a shape such that it has a size enough to cover said tunnel film and has a gate length approximately equal to a length of said channel region between said drain region and said source region;

an interlayer insulating film covering an upper face and side faces of said floating gate electrode; and

a control gate electrode formed above said floating gate electrode interposing said interlayer insulating film therebetween.

2. The EEPROM as claimed in claim 1, wherein said control gate

electrode is shaped to be wider than said floating gate electrode and to wrap said floating gate electrode above said tunnel film and is shaped to be narrower than said floating gate electrode above said channel region.

3. The EEPROM as claimed in claim 1, wherein said floating gate electrode and said control gate electrode each have an opening and the position of the opening in the control gate electrode offsets toward said channel region so that said control gate electrode wraps said floating gate electrode above said tunnel film and is narrower than said floating gate electrode above said channel region.

4. An EEPROM of a floating gate type and a two-layer polysilicon type having a memory transistor and a select transistor for selecting said memory transistor, said memory transistor comprising:

an embedded layer of a second conductivity type formed in a superficial layer of a semiconductor substrate of a first conductivity type;

a drain side field moderating layer of the second conductivity type formed adjacent to said embedded layer in the superficial layer of said semiconductor substrate;

a source region of the second conductivity type in the superficial layer of said semiconductor substrate;

a channel region between said drain side field moderating layer and said source region;

a gate insulating film formed on a surface of said semiconductor substrate;

a tunnel film formed in a part of said gate insulating film above said embedded layer;

a floating gate electrode formed above said tunnel film and said channel region and having a shape such that it entirely covers said tunnel film and covers neither said source region nor said drain side field moderating layer;

an interlayer insulating film covering an upper face and side faces of said floating gate electrode; and

a control gate electrode formed above said floating gate electrode interposing said interlayer insulating film therebetween,

wherein said source region and said drain side field moderating layer are self-aligningly formed by ion implantation using said floating gate electrode as a mask, and

wherein said control gate electrode is shaped to be wider than said floating gate electrode and to wrap said floating gate electrode above said tunnel film and is shaped to be narrower than said floating gate electrode above said channel region.

5. The EEPROM as claimed in claim 4, wherein said select transistor has a gate electrode and a source region, the EEPROM further comprising a source side field moderating layer of the second conductivity type in at least one of source regions of said memory transistor and said select transistor, said source side field moderating layer being self-aligningly formed by ion implantation using said floating gate electrode or said gate electrode as a mask.

6. The EEPROM as claimed in claim 5, further comprising a source

layer of the second conductivity type offset against said source side field moderating layer and having a higher concentration than said source side field moderating layer, so that at least one of said memory transistor and said select transistor has an offset type source structure.

7. The EEPROM as claimed in claim 4, wherein said select transistor has a gate electrode formed simultaneously with said floating gate electrode of said memory transistor from a first polysilicon layer.

8. The EEPROM as claimed in claim 4, wherein said select transistor has a drain side field moderating layer in a drain region, said drain side field moderating layer being formed simultaneously with said drain side field moderating layer of said memory transistor and self-aligningly by ion implantation using said gate electrode as a mask.

9. The EEPROM as claimed in claim 4, wherein said interlayer insulating film includes a nitride film and is formed on said semiconductor substrate including a surface of said gate electrode in a whole region of said select transistor and said memory transistor.

10. The EEPROM as claimed in claim 4, further comprising an insulation film for element separation formed on the surface of said semiconductor substrate, wherein a length of a region where said tunnel film is formed is regulated by said insulation film.

11. A manufacturing method of a floating gate type EEPROM having a memory transistor and a select transistor for selecting said

memory transistor, said manufacturing method comprising the steps of:

forming an embedded layer of a second conductivity type in a region where said memory transistor is to be formed in a semiconductor substrate of a first conductivity type;

forming a gate insulating film on a surface of said semiconductor substrate in which said embedded layer has been formed;

exposing the surface of said semiconductor substrate through said gate insulating film by etching a part of said gate insulating film on said embedded layer;

forming a tunnel film on the exposed surface of said semiconductor substrate;

forming a floating gate electrode by forming a first polysilicon layer on said gate insulating film and said tunnel film and then patterning it, said floating gate electrode having a shape such that it covers the entirety of said tunnel film and a channel formation region where a channel region is to be formed and does not cover a region between said channel formation region and said embedded layer and a source formation region where a source region is to be formed;

forming a drain side field moderating layer of the second conductivity type adjacently to said embedded layer and self-aligningly by implanting ions into the region between said channel formation region and said embedded layer with said floating gate electrode used as a mask;

forming an interlayer insulating film so as to entirely

cover an upper face and side faces of said floating gate electrode;

forming a control gate electrode by forming a second polysilicon layer on said interlayer insulating film in a state where said interlayer insulating film entirely covers the upper face and side faces of said floating gate electrode and then patterning it, said control gate electrode having a shape such that, above said tunnel film, it is wider than said floating gate electrode and wraps said floating gate electrode, and, above said channel formation region, it is narrower than said floating gate electrode and does not cover said drain side field moderating layer; and

forming a source region self-aligningly by implanting ions into a superficial layer of said semiconductor substrate with said floating gate electrode used as a mask so that said channel region is formed between said drain side field moderating layer and said source region.

12. The manufacturing method as claimed in claim 11, further comprising the steps of:

forming a gate electrode on a surface of said semiconductor substrate in a region where said select transistor is to be formed;

forming a source region in the superficial layer of said semiconductor substrate adjacently to said embedded layer and self-aligningly by implanting ions with said gate electrode used as a mask; and

forming a source side field moderating layer of the second conductivity type by ion implantation using said floating gate electrode or said gate electrode as a mask in at least one of

the steps of forming said source regions of said memory transistor and said select transistor.

13. The manufacturing method as claimed in claim 12, wherein the step of forming said drain side field moderating layer of said memory transistor and the step of forming said source side field moderating layer are carried out simultaneously under the same ion implantation conditions.

14. The manufacturing method as claimed in claim 12, wherein in the step of forming said source region, a source layer of the second conductivity type is formed to be offset against said source side field moderating layer and to have a higher concentration than said source side field moderating layer.

15. The manufacturing method as claimed in claim 11, wherein in the step of forming said floating gate electrode, said gate electrode of said select transistor is formed simultaneously with said floating gate electrode by patterning said first polysilicon layer.

16. The manufacturing method as claimed in claim 11, further comprising the step of forming a drain side field moderating layer in a region where a drain region of said select transistor is to be formed,

wherein said drain side field moderating layer is formed simultaneously with said drain side field moderating layer of said memory transistor and self-aligningly by ion implantation using said gate electrode as a mask under the same ion implantation conditions as said drain side field moderating layer of said memory transistor.

17. The manufacturing method as claimed in claim 11, wherein, in the step of forming said interlayer insulating film, said interlayer insulating film having a nitride film and is formed on said semiconductor substrate including a surface of said gate electrode in whole regions of said select transistor and said memory transistor, and wherein said EEPROM is manufactured in a state where said interlayer insulating film remains in the whole regions of said select transistor and said memory transistor.